



Serial No. 09/648,164

IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE

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Patent Application

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Monroe, Donald

Case: **15-6-9**

Serial No.: **09/648164**

Filing Date: **August 25, 2000**

Examiner: **Dickey**

Group Art Unit: **2826**

Title: **Architecture for Circuit Connection Of A Vertical Transistor**

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks Washington, D.C. 20231 on **2-13-03**

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SIR:

Amendment Under 37 C.F.R. §1.111

In response to the office action of October 22, 2002, please amend the above-identified application as follows:

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IN THE CLAIMS

- 31
1. (Amended) An integrated circuit structure comprising:
a semiconductor layer having a major surface formed along a plane;
first and second spaced-apart doped regions extending into the surface from the plane;
a third doped region of different conductivity type than the first region, positioned above the plane and over the first region; and
a conductive layer formed between the first and second regions and above the plane, providing electrical connection between the doped regions.

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